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**UNITED STATES DEPARTMENT OF COMMERCE**  
**Patent and Trademark Office**

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Washington, D.C. 20231

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
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09/351,160 07/12/99 NISHIJIMA M 0819-261

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MMC1/0929

OWENS, D

2811

EXAMINER

ART UNIT

PAPER NUMBER

DATE MAILED:  
09/29/00

Please find below and/or attached an Office communication concerning this application r  
proceeding.

Commissioner of Patents and Trademarks

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# Office Action Summary

Application No.

09/351,160

Applicant(s)

NISHIJIMA, MASAOKI

Examiner

Douglas W Owens

Art Unit

2811

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

## Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).

## Status

- 1) ☐ Responsive to communication(s) filed on \_\_\_\_.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

## Disposition of Claims

- 4) ☒ Claim(s) 1-22 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-22 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_ is/are objected to.
- 8) ☐ Claims \_\_\_\_ are subject to restriction and/or election requirement.

## Application Papers

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 12 July 1999 is/are objected to by the Examiner.
- 11) ☐ The proposed drawing correction filed on \_\_\_\_ is: a) ☐ approved b) ☐ disapproved.
- 12) ☐ The oath or declaration is objected to by the Examiner.

## Priority under 35 U.S.C. § 119

- 13) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).
- a) ☒ All b) ☐ Some \* c) ☐ None of the CERTIFIED copies of the priority documents have been:
1. ☒ received.
2. ☐ received in Application No. (Series Code / Serial Number) \_\_\_\_.
3. ☐ received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

- 14) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. & 119(e).

## Attachment(s)

- 15) ☒ Notice of References Cited (PTO-892)
- 16) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 17) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 5,7.
- 18) ☐ Interview Summary (PTO-413) Paper No(s). \_\_\_\_.
- 19) ☐ Notice of Informal Patent Application (PTO-152)
- 20) ☐ Other: \_\_\_\_\_

## DETAILED ACTION

### *Drawings*

1. Figures 10-12 and 13-16 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g).

### *Specification*

2. The disclosure is objected to because of the following informalities:  
  
in line 22 of page 4, "inductor" is misspelled "indictor";  
  
in line 6 of page 6, "Figures" should be replaced with "Figure".  
  
Appropriate correction is required.

### *Claim Rejections - 35 USC § 102*

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

4. Claims 9-15 and 19-22 are rejected under 35 U.S.C. 102(e) as being anticipated by Weigand et al., US patent No. 6,046,503.

Regarding claims 9, 11 and 13, Weigand et al. teaches a semiconductor device with a line structure, wherein the line structure comprises:  
  
a conductor layer (12/18);  
  
a first dielectric film (20,22) on the conductor layer;  
  
a conductor line (40) on the first dielectric film;

a second dielectric film (20',22') covering the conductor line; and  
wherein a region of the conductor layer, has been partially removed.

Regarding claims 10 and 12, Weigand et al. teaches a semiconductor device, wherein the first dielectric film includes two dielectric layers with different dielectric constants.

Regarding claim 14, Weigand et al. teaches a semiconductor device, wherein the dielectric constant of the dielectric layer over the conductor line is greater than 10.

Regarding claims 15 and 22, Weigand et al. teaches a semiconductor device further comprising an RF operable active component on the substrate and electrically connected to the line structure (Col. 3 lines 25-32).

Regarding claim 19, Weigand et al. teaches a semiconductor device with a line structure, wherein the line structure comprises:

a first dielectric film (20,22) on the substrate;  
a coplanar conductor layer (40) on the first dielectric film; and  
a second dielectric film (20',22') on the coplanar conductor layer.

Regarding claim 20, Weigand et al. teaches a semiconductor device, wherein the dielectric constant of first dielectric film (22) is greater than 10.

Regarding claim 21, Weigand et al. teaches a semiconductor device, wherein the first dielectric film comprises two layers with different dielectric constants.

***Claim Rejections - 35 USC § 103***

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

Art Unit: 2811

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

6. Claims 1-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bartelink, US patent No. 5,567,982.

Regarding claims 1, 4, 6, 7, 9 and 10, Bartelink teaches a semiconductor device with a line structure, wherein the line structure comprises:

a dielectric film comprising a first dielectric portion (408), and second and third dielectric portions (410) disposed laterally to sandwich the first dielectric portion therebetween;

wherein the dielectric constant of the first dielectric portion is different from that of the second and third dielectric portions; and

a conductor line (414) on the dielectric layer.

Bartelink does not teach a semiconductor device including a conductor layer on the substrate. Admitted prior art teaches a conductive grounding layer on the substrate. It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the conductive grounding layer of admitted prior art into the device taught by Bartelink, since it is desirable to provide a ground plane for microwave circuits.

Bartelink does not explicitly teach semiconductor device further comprising another dielectric film over the conductor line. It is conventional in the art to provide passivation layers over conductive structures of semiconductor devices. It would have been obvious to one of ordinary skill in the art to employ conventional structures, since it

is desirable to provide a planarized surface for additional structures, as well as preventing shorting between conductive structures.

Regarding claim 2, Bartelink teaches a semiconductor device, wherein the dielectric constant of the first dielectric portion is lower than the dielectric constant of second and third dielectric portions.

Regarding claim 3, neither Bartelink nor admitted prior art teach a dielectric material for the second and third portions, wherein the dielectric constant is higher than 10. The examiner takes official notice that there are many dielectric materials that have a dielectric constant that is greater than 10. It would have been obvious to one of ordinary skill in the art to select one of these materials as a matter of design choice.

Regarding claim 5, Bartelink does not explicitly teach active components formed on the substrate and connected to the line structure. Admitted prior art teaches active components connected to the line structure. It would have been obvious to one of ordinary skill in the art to connect the line structures to active elements since it is desirable for active elements to communicate with other devices on the substrate.

Regarding claim 8, Bartelink teaches a semiconductor device, wherein at least one of the dielectric layers has been patterned.

7. Claims 16-18, and 20-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wakimoto et al. in view of Weigand et al.

Regarding claim 16, Wakimoto et al. teaches a semiconductor device with a line structure, wherein the line structure comprises:

a coplanar conductor layer comprising a grounded conductor layer (20a, 20b) and a conductor line (36-2) spaced apart from the grounded conductor layer.

Wakimoto et al. does not teach a semiconductor device wherein the dielectric film has a dielectric constant greater than 10. Weigand et al. teaches a semiconductor device, wherein the dielectric film (22) has a dielectric constant greater than 10. It would have been obvious to one of ordinary skill to incorporate the dielectric film taught by Weigand et al. into the device taught by Wakimoto et al. since it is desirable to protect the underlying dielectric layer during patterning of metal layers.

Regarding claim 17, Wakimoto et al. teaches a semiconductor device, wherein the dielectric constant of the dielectric film between the grounded conductor layer and the conductor line is less than 10.

Regarding claim 18, Wakimoto et al. does not explicitly teach a semiconductor device further comprising an active RF operable component connected to the line structure. Wakimoto et al. teaches a wiring structure for use with active devices (Col. 1, lines 17-31). It is inherent that active devices would have been formed on the substrate since the device taught by Wakimoto et al. is for use with active components.

### ***Conclusion***

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Dougherty et al., US patent No. 5,194,833. Fukuta et al., US patent No. 4,751,482. Ma, US patent No. 5,729,047. Kobayashi, US patent No. 5,357,138.

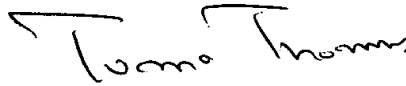


Any inquiry concerning this communication or earlier communications from the examiner should be directed to Douglas W Owens whose telephone number is 703-308-6167. The examiner can normally be reached on Monday-Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on 703-308-2772. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7722 for regular communications and 703-308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

DWO  
September 27, 2000

  
Tom Thomas  
Supervisor, Examination  
Technical Center 2000